

What Is Claimed Is:

1. An address generator comprising:
 - an adder to add a first address component and a second address component to generate an address;
 - a correction indicator to indicate if the address is correct; and
 - a control input to modify an operation of the adder.
2. An address generator as defined in claim 1 wherein the operation of the adder comprises determining a carry bit.
3. An address generator as defined in claim 2 wherein the control input modifies the operation of the adder to force the carry bit to be equal to one of a logic ZERO and a logic ONE.
4. An address generator as defined in claim 1 wherein the correction indicator generates a control output based on a set of carry bits in the adder.
5. An address generator as defined in claim 4 wherein the correction indicator generates the control output based on an exclusive OR operation performed on the set of carry bits.

6. An address generator as defined in claim 1 wherein the control input is a first control input, and further comprising a second control input to specify a size of the address.
7. An address generator as defined in claim 6 wherein the adder blocks a set of carry bits in the adder based on the second control input.
8. An address generator as defined in claim 6 wherein the correction indicator generates a control output based on the second control input.
9. An address generator as defined in claim 1 wherein the adder comprises a first adder and a second adder, and wherein the correction indicator generates a control output based on a first set of carry bits in the first adder and a second set of carry bits in the second adder.
10. An address generator as defined in claim 9 wherein the correction indicator generates the control output based on an exclusive OR operation performed on the first set of carry bits and the second set of carry bits.

11. An apparatus comprising:

an instruction scheduler to schedule a set of address components to process;

an address generator to generate a first address from the set of address components; and

a recovery unit to determine whether the first address is correct, and to modify an operation of the address generator to cause the address generator to generate a second address from the set of address components if the first address is incorrect.

12. An apparatus as defined in claim 11 wherein the address generator comprises an adder to generate one of the first address and the second address by adding the set of address components.

13. An apparatus as defined in claim 12 wherein the address generator further comprises a control input to modify an operation of the adder.

14. An apparatus as defined in claim 13 wherein the operation comprises determining a carry bit.

15. An apparatus as defined in claim 14 wherein the control input modifies the operation to force the carry bit to be equal to one of a logic ZERO and a logic ONE.

16. An apparatus as defined in claim 13 wherein the recovery unit sets the control input to a value if the first address is incorrect.
17. An apparatus as defined in claim 16 wherein the value is based on a previous value of the control input.
18. An apparatus as defined in claim 13 wherein the instruction scheduler sets the control input to a value.
19. An apparatus as defined in claim 11 wherein the address generator further comprises a control output, and wherein the recovery unit determines whether the first address is correct based on the control output.
20. An apparatus as defined in claim 19 wherein the address generator further comprises an adder to generate one of the first address and the second address by adding the set of address components, and wherein the control output is based on a set of carry bits in the adder.

21. An apparatus as defined in claim 13 wherein:

the address generator further comprises a first control output and a second control output;

the recovery unit determines whether the first address is correct based on the first control output; and

the recovery unit sets the value of the control input based on the second control output.

22. An apparatus as defined in claim 21 wherein the second control output of the address generator is based on a previous value of the control input.

23. An apparatus as defined in claim 13 wherein the control input is a first control input, and wherein the address generator further comprises a second control input to specify a size of the address.

24. An apparatus as defined in claim 23 wherein the adder blocks a set of carry bits in the adder based on the second control input.

25. An apparatus as defined in claim 23 wherein the address generator further comprises a control output, and wherein the control output is based on the second control input.

26. An apparatus as defined in claim 11 wherein the instruction scheduler, the address generator and the recovery unit are located in a processor, and further comprising a dynamic random access memory coupled with the processor.
27. A method of generating an address in a processor comprising:
 - performing a first addition of a first address component and a second address component to generate a first address;
 - determining whether the first address is correct; and
 - modifying an operation in a second addition of the first address component and the second address component to generate a second address if the first address is incorrect.
28. A method as defined in claim 27 wherein the operation comprises determining a carry bit.
29. A method as defined in claim 28 wherein modifying the operation comprises forcing the carry bit to a value.
30. A method as defined in claim 29 wherein the value is one of a logic ZERO and a logic ONE.

31. A method as defined in claim 29 wherein the value is based on a previous value of the carry bit.
32. A method as defined in claim 29 wherein the value is based on at least one of the first address component and the second address component.
33. A method as defined in claim 27 wherein determining whether the first address is correct comprises evaluating a set of carry bits in the first addition of the first address component and the second address component.
34. A method as defined in claim 33 wherein determining whether the first address is correct comprises performing an exclusive OR operation on the set of carry bits.
35. A method as defined in claim 27 wherein determining whether the first address is correct is based on a size of one of the first address and the second address.
36. A method as defined in claim 35 wherein the size is one of a first size and a second size.

37. A method as defined in claim 27 wherein performing one of the first addition and the second addition comprises modifying an operation in the one of the first addition and the second addition.
38. A method as defined in claim 37 wherein the operation comprises determining a set of carry bits, and wherein modifying the operation comprises forcing a bit in the set of carry bits to a value.
39. A method as defined in claim 38 wherein the value is one of a logic ZERO and a logic ONE.
40. A method as defined in claim 37 wherein modifying the operation is based on a size of the one of the first address and the second address.
41. A method as defined in claim 40 wherein the size is one of a first size and a second size.